REMARKS/ARGUMENTS

Claims 31-42 are pending. Claims 31 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Rosen et al., U.S. Patent No. 6,272,595. Claims 35 and 40-42 are rejected under U.S.C. 103(a) as being unpatentable over Rosen et al., U.S. Patent No. 6,272,595 and Kumar et al., U.S. Patent No. 6,922,745.

First, Applicants gratefully acknowledge the Office Action's indication claims 32-34 and 37-39 contain allowable subject matter. *See* Office Action 2/3/2006, page 6.

Applicants assert the cited references do not teach, suggest, or describe at least "[a] multiple store buffer forwarding apparatus, comprising...a non-volatile memory coupled to the processor...[to] cause the processor to ... execute *a load instruction referencing a second memory* region; determine that *the second memory region* matches a cacheline address..." (e.g., as described in claim 31).

The Office Action asserts Rosen teaches executing a load instruction referencing a second memory region at column 4, lines 40-43 and column 5, lines 17-23 and determining that the second memory region matches a cacheline address at column 5, lines 17-23. *See* Office Action dated 2/3/2006, page 3. Applicants disagree.

Column 4, lines 40-43 state: "The store hit buffer 200 buffers each write operation received from the processor 222 over the data bus 16 and address bus 18."

Applicants maintain the sections cited by the Office Action are inadequate for at least two reasons: a) they do not discuss *load instructions* ; and b) they do not discuss instructions referencing a *memory region* at all (or a "second memory region"). First, the cited section describes *processor 222* sending write operation data over data and address buses to *a buffer* 200. Clearly, this is not a *load instruction*. Second, the data does not reference a memory region

(or a "second memory region" as described in claim 31) at all, but *processor* 222. Applicants submit for at least these reasons, the cited section does not describe executing *a load instruction referencing a second memory region* at all.

Next, column 5, lines 17-23 state:

> If the set address 90 for a read operation to the cache memory 10 matches the buffered set address 162 for the cache line bit stored in the write buffer circuit 120, then the set compare result 164 causes one of the 2:1 multiplexers 110-113 to select the buffered data bit 166. The selected data bit is transferred to the four way multiplexer 115 over a set of 2:1 mux data lines 170-173.

This section fails to support a proper rejection for at least the reasons describe above. It describes a "match" operation (as part of and for a *read operation*), wherein the set address of a cache memory 10 is compared to cache bit line of a write buffer circuit 120. It does not describe a) a *load operation* or b) executing a load instruction referencing a second memory region as described in claim 31. The remaining portion of the cited section is inapplicable and inadequate to support a proper rejection as well as it describes the consequences of this "*match operation.*"

Moreover, Applicants submit even if the Office Action's arguments were assumed to be true *arguendo,* the cited section column 5, lines 17-23 fails to describe determining that the second memory region matches a cacheline address. Presumably, the Office Action utilizes this section to argue the set address 90 of a cache memory 10 is compared to the buffered set address 162 of write buffer circuit 120.

However, in its citation regarding the "first memory region" and the "second memory region" limitations, the Office Action presumably cites to the cache memory 10 as being the first memory (*citing* column 4, lines 55-64) and *the store hit buffer 200* as being the second memory region (see column 4, lines 40-43 – quoted above). *See* id. For at least the reasons discussed

above, Applicants maintain the instructions are sent from processor 222, not from the store hit buffer 200 (nor a memory region of any sort). However, assuming *arguendo* the instructions *were* from store hit buffer 200, Applicants submit the Rosen reference still does not describe at least a cacheline address of this store hit buffer 200 (the alleged "second memory region") being matched to anything. In order to support a proper rejection, the Rosen reference must describe at least a first memory region, a second memory region, and a matching determination with regard to the cacheline of the cited second memory region, as described in embodiments of the present application. It does not.

Kumar fails to make up for the deficiencies of Rosen. Kumar is directed toward locked-load instructions; specifically determining an attribute of a locked load instruction and selecting a lock protocol based on said attribute. It is not directed toward the execution of load instructions as described in the embodiments of the present application.

Therefore, since each and every limitation is not taught or suggested in the cited references, Applicants submit they are inadequate to support proper 35 U.S.C. §102(b) rejections, independent claim 31 should be allowed. Independent claims 36 and 41 include similar limitations, and therefore are also in condition for allowance. Claims 32-35, 37-40 and 42 depend from allowable independent claims and therefore are allowable as well.

For at least all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited. The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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